TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC's

This application is a continuation-in-part application of serial number 10/058,259, filed on Jan. 29, 2002, which is a continuation application of serial number 09/251,183, filed on February 17, 1999, now issued as US Patent 6,383,916, which is a continuation-in-part application of serial number 09/216,791, filed on December 21, 1998.

BACKGROUND OF THE INVENTION

(1) Field of the invention.

The invention relates to the manufacturing of high performance Integrated Circuit (IC's), and more specifically to methods of achieving high performance of the Integrated Circuits by reducing the parasitic capacitance and resistance of inter-connecting wiring on chip.

(2) Description of the Prior Art.

When the geometric dimensions of the Integrated Circuits are scaled down, the cost per die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance

and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines. Increased Input-Output (IO) combined with increased demands for high performance IC's has led to the development of Flip Chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads on chip and interconnect the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges. In mounting several packages together, such as

surface mounting a ceramic package to a plastic board, the TCE mismatch can cause a large thermal stress on the solder-lead joints that can lead to joint breakage caused by solder fatigue from temperature cycling operations.

US 5,212,403(Nakanishi) shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

US 5,501,006(Gehman, Jr. et a].) shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

US'5,055,907(Jacobs) discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film multi-layer wiring decal on the support substrate and over the chip. However, this reference differs from the invention.

US 5,106,461 (Volfson et al.) teaches a multi layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

US 5,635,767(Wenzel et al.) teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

US 5,686,764(Fulcher) shows a flip chip substrate that reduces RC delay by separating the power and 1/0 traces.

SUMMARY OF THE INVENTION

It is the primary objective of the present invention to improve the performance of High Performance Integrated Circuits.

Another objective of the present invention is to reduce resistive voltage drop of the power supply lines that connect the IC to surrounding circuitry or circuit components.

Another objective of the present invention is to reduce the RC delay constant of the signal paths of high performance IC's.

Yet another objective of the present invention is to facilitate the application of IC's of reduced size and increased circuit density.

Yet another objective of the present invention is to further facilitate and enhance the application of low resistor conductor metals..

Yet another objective of the present invention is to allow for increased I/O pin count for the use of high performance IC's.

Yet another objective of the present invention is to simplify chip assembly by reducing the need for re-distribution of I/O chip connections.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to power buses.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to clock distribution networks.

Yet another objective of the present invention is to reduce IC manufacturing costs by allowing or facilitating the use of less expensive process equipment and by accommodating less strict application of clean room requirements, this as compared to sub-micron manufacturing requirements.

Yet another objective of the present invention is to be a driving force and stimulus for future system-on-chip designs since the present invention allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

Yet another objective of the present design is to form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

The present invention adds one or more thick layers of polymer dielectric and one or more layers of thick, wide metal lines on top of the finished device wafer passivation. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 um. The wide metal lines can, for instance, be of electroplated copper or gold. These layers of dielectric and metal lines are of primary benefit for long signal paths and can also be used for power buses or power planes, clock distribution networks, critical signal, re-distribution of I/O pads for flip chip applications. Single, dual and triple damascene techniques, or combinations thereof, are used for forming the metal lines and via fill.

Furthermore, a method for forming a post-passivation, top metallization system for high performance integrated circuits is provided. An integrated circuit is provided, having devices formed in and on a semiconductor substrate. An overlaying fine line interconnecting metallization structure with first metal lines is connected to the devices, and has a passivation layer formed thereover, with first openings in the passivation layer to contact pads connected to the first metal lines. A top metallization system is formed above the passivation layer, connected to the interconnecting metallization structure, wherein the top metallization system has top metal lines, in one or more layers, having a width substantially greater than the first metal lines, and wherein the top metallization system connects portions of the interconnecting metallization structure to other portions of the interconnecting metallization structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a-1b show a cross section of the interconnection scheme of the present invention.

Fig. 2 shows a cross section of the present invention in a more complex circuit configuration.

Fig. 3a shows the top view of a combination power and X-signal plane using the present invention.

Fig. 3b shows the top view of a combination power and Y-signal plane using the present invention.

Fig. 4 shows the top view of solder bump arrangement using the present invention and is an expanded view of a portion of Fig. 5.

Fig. 5 shows the top view of an example of power/ground pads combined with signal pad using the present invention.

Fig. 6 shows a basic integrated circuit (IC) interconnect scheme of the invention.

Fig. 7 shows an extension of the basic IC interconnect scheme by adding power, ground and signal distribution capabilities.

Fig. 8 shows an approach of how to transition from sub-micron metal to wide metal interconnects.

Fig. 9 shows detail regarding BGA device fan out using the invention.

Fig. 10 shows detail regarding BGA device pad relocation using the invention.

Fig. 11 shows detail regarding the usage of common power, ground and signal pads for BGA devices using the invention.

Figs. 12a-12h shows a method for transitioning from a fine-line interconnection to the post passivation interconnection of the invention, and one method for forming the post passivation interconnection.

Figs. 13-21 show a method for forming the thick, wide metal lines, and via fill, of the invention, using a dual damascene technique.

Figs. 22-27 show a method for forming the thick, wide metal lines, and via fill, of the invention, using a triple damascene technique.

Fig. 28 shows an embodiment of the invention in which a first metal layer of the invention is deposited directly on the passivation layer.

Figs. 29-35 show another embodiment of the invention in which the top metal system of the invention is formed by deposition and etching.

DETAILED DESCRIPTION OF THE INVENTION

The present invention teaches an Integrated Circuit structure where key re-distribution and interconnection metal layers and dielectric layers are added over a conventional IC. These re-distribution and interconnection layers allow for wider buses and reduce conventional RC delay.

Fig. 1a shows a cross-sectional representation of a general view of the invention. Devices 2 are formed in and on a semiconductor substrate 1, and metallization is accomplished in one or more layers of IC Interconnection 3, above the device layer. The IC interconnection connects the devices to one another to form operational circuits, and also has in its top layer of metal points of electrical contact (such as bond pads), which provide connections from the IC interconnection layer to outside of the IC. A passivation layer 4 covers the IC interconnection scheme, while providing openings to the electrical contact points.

In a key aspect of the invention, the passivation openings can be as small as 0.1 um. In another critical aspect of the invention, various methods are used to form the Post Passivation Technology segment 80, in which metal lines which are formed substantially thicker and wider than those in the IC Interconnection layer. More detail is provided below.

Referring now more specifically to Fig. 1b, there is shown a cross section of one implementation of the present invention. A silicon substrate 1 has transistors and other devices, typically formed of polysilicon, covered by a dielectric layer 2 deposited over the devices and the substrate. Layer 3 indicates the totality of metal layers and dielectric layers that are typically created on top of the device layer 2. Points of contact 6, such as bonding pads known in the semiconductor art, are in the top surface of layers 3 and are part of layer 3. These points of contact 6 are points within the IC arrangement that need to be further connected to surrounding circuitry, that is to power lines or to signal lines. A passivation layer 4, formed of for example silicon nitride, is deposited on top of layer 3, as is known in the art for protecting underlying layers from moisture, contamination, etc.

The key steps of the invention begin with the deposition of a thick layer 5 of a polymer. A pattern 7 is exposed and etched through the polymer layer 5 and the passivation layer 4 where the pattern 7 is the same as the pattern of the contact points 6. This opens the contact points 6 up to the surface 8 of the polymer layer 5.

In one important aspect of the current invention, referring now to Figs. 12a-12h, and specifically Fig. 12a, openings 7 in the polymer layer 5 may be larger than openings 7' in the passivation layer 4. Openings 7' may be formed to as small as 0.1 um, and may range in size from between about 0.1 and 50 um. These small passivation vias 7' are advantageous for the following reasons:

(1) small passivation vias only need small underlying metal pads (or dog bone structures); and these small metal pads will not block the routing capability of the top layer metal in the IC fine line interconnection scheme.

(2) Since the thickness of the inter-metal-dielectric (IMD) in the IC fine line interconnection is thin, a small metal pad is needed to provide small capacitance.

Electrical contact with the contact points 6 can now be established by filling the openings 7 (and 7') with a conductor. Simultaneously with filling of the openings 7, a first interconnect metal layer may be formed, as shown in Fig. 12a. This thick metal layer is formed by first sputtering an adhesion layer 200. The adhesion layer is formed of titanium tungsten (TiW), chromium (Cr), titanium (Ti), palladium (Pd), nickel (Ni) or titanium nitride (TiN), and is deposited to a thickness of between about 0.01 and 3 microns. An electroplating seed layer 202 is then deposited by sputtering, the seed layer material being copper (Cu), gold (Au), palladium (Pd) or nickel (Ni), formed to a thickness of between about 0.05 and 3 microns, as shown in Figs. 12b and 12c. Pd is

used as the seed layer when gold is to be electroplated, and Ni used as the seed layer for plating nickel. A thick photoresist 203, as depicted in Fig. 12d, of between about 2 and 100 microns thickness, is next deposited and patterned over the seed layer. A thick layer of metal, such as copper (Cu), gold (Au), palladium (Pd) or nickel (Ni), is then electroplated to a thickness of between about 2 and 100 microns, as shown in Fig. 12e, to form thick metal interconnections 204 and to fill openings 7. Referring now to Fig. 12f and 12g, the photoresist is then stripped, and portions of the seed metal and adhesion metal removed, using the thick metal as an etch mask.

Where Cu is used for electroplating to form the structure of Fig. 12g, a nickel cap layer (not shown) may be used to prevent copper corrosion and to prevent interaction of the copper with the surrounding polymer.

Subsequent metal layers may be formed in a similar manner to that shown for the first metal layer in Figs. 12a-g. For example, referring to Fig. 12h, another thick polymer layer is deposited over the interconnect line 204 and an opening 223 formed for connection of the next metal layer to the first metal layer. Adhesion and electroplating seed layers are then sputtered, a thick photoresist deposited and the next thick metal layer electroplated, etc.

The thick metal 204 of the post passivation process of the invention is thicker then the typical fine-line metal layers 3 by a ratio of between about 2 and 1000 times. The thick metal layers are formed into interconnecting lines that also are wider than the

fine-line metal by a ratio of between about 2 and 1000 times. Thicker, wider metal in the post-passivation process of the invention reduces the resistance of these interconnections.

Alternately, the opening 7 may be filled with a metal plug, formed of, for example, tungsten, and then thick metal formed to contact the via plug, using the above described electroplating process.

In one embodiment of the invention, polymer layer 5 may be omitted, with the thick metal layer formed directly on passivation layer 4 and connecting to the underlying metal pads.

In one variation of the above-described process for forming the thick metal layers, damascene processes may be used, as shown in Figs 13-27. Please refer first to Figs. 13-21, in which a dual damascene technique for forming 2 vias, followed by a single damascene method for forming interconnecting lines, is shown. Openings 7 and 7' are formed as previously described, in polymer layer 5 and passivation layer 4, respectively. Opening 7, and subsequent openings in the polymer layers of the top metallization system, can be formed in one of two ways. In a first, preferred method, polymer 5 (and subsequent polymer layers) is formed of a photosensitive polymer material, such materials being known in the art. Such photosensitive polymers can be exposed and developed directly using photolithography. Alternatively, a non-photosensitive polymer is used, and patterned using photoresist and known

photolithography techniques. The former method is preferred due to the savings in materials cost, from not having to use thick layers of photoresist, which is expensive.

An adhesion layer 200 and an electroplating seed layer 202 are now formed, also as previously described with reference to Fig. 12a, and as shown in Fig. 13. Copper or gold 210 is electroplated up from seed layer 202 to fill openings 7' and 7, as well as above polymer layer 5, as depicted in Fig. 15. Chemical mechanical planarization (CMP) is used to remove the plated metal 210 above polymer 5, stopping on seed layer 202. This forms via plugs 212 above and connecting to contact points 6, as shown in Fig. 16. Via plugs 212 have a width of between about 1 and 300 um.

Referring now to Figs. 17-21, polymer 214 is deposited and patterned to create interconnecting line opening 215, for the purposes of interconnecting two or more contact points 6 of the fine-line metallization system, using a single damascene method. In a similar manner as previously described, an adhesion layer and electroplating seed layer 216 are sputtered. Metal 218 is electroplated to fill line opening 215, and then planarized back, as shown in Figs. 18-20. Thus thick interconnecting metal line 221 is formed, connecting two or more contact points 5, and having all the advantages of the invention herein described – thick, wide metal having low resistance and capacitance, and other advantages to be further described below.

Further layers of the upper metal scheme may subsequently be formed. First, another polymer layer 222 is deposited and patterned to form via 223. Two alternatives

may then be used to fill the via and form interconnecting lines. First, a dual damascene method is used, such as partially shown in Fig. 21b, in which a second polymer layer 224 is deposited and patterned to form interconnecting line opening 225. Subsequent processing (not shown) then takes place, as described above, by forming adhesion and seed layers, plating, and CMP. The second method is partially shown in Fig. 21c, in which via 223 is first filled with adhesion and seed layers 226, and then via metal is electroplated and planarized using CMP. Then second polymer 224 is deposited, and patterned as shown, and then filled with metal and planarized, to form interconnecting lines (not shown).

The above described damascene techniques provide excellent planarity, and particularly when photosensitive polymer is used, is very cost-effective.

Figs. 22-27 depict a triple damascene process for forming the first metal system above passivation 4. Starting from the configuration shown in Fig. 13, a photoresist or other photosensitive polymer 230 is deposited to fill openings 7 and 7', as well as above polymer 5. This layer is patterned using conventional lithography and etching to form opening 232, as shown in Fig. 23. Adhesion layer and electroplating seed layer (shown as a single layer 234) are sputtered as previously described, as depicted in Fig. 24, followed by gold or copper plating 236, in Fig. 25. CMP is used to planarize back the plated layer, and this simultaneously forms via plugs 212 and thick, wide interconnection 221. Subsequent additional layers of metal may then be formed, after

deposition of polymer layer 238 and formation of opening 240, etc, shown in Fig. 27, by using the techniques described above with reference to Figs. 21b-21c.

In another embodiment of the invention, the first metal lines of the invention top metallization system may be formed directly on passivation layer 4, as partially shown in Fig. 28. A dual damascene technique may be used to fill via 7' and line opening 252, within polymer layer 250. Metallization is performed similarly to that discussed above and so will not be further described in detail.

An alternative to using the above-described damascene techniques for metallization of the top metal system of the invention is to use a metal deposition and etch, as shown in Figs. 29-35. In one embodiment, pure aluminum Al is blanket sputtered and patterned, as is known in the art, to form vias and interconnecting lines. Patterning can be by dry or wet etching. Copper Cu, nickel Ni, or gold Au may also be blanket sputtered instead of aluminum Al, using an underlayer of titanium (Ti), titanium tungsten (TiW) or chromium (Cr) (as an adhesion and barrier layer), and then patterned by wet etching. The detailed process is shown starting in Fig. 30, in which the adhesion layer 300 is sputtered into via 7 and 7', to contact the pad 6, and covers (optional) polymer layer 5. In Fig. 30, the bulk metal 302 (Au, Cu or Ni) is sputtered over the adhesion layer (or in the case of Al, blanket sputtering is used without the adhesion layer), to fill vias 7 and 7' and to a thickness sufficient to form metal interconnecting lines, between 2 and 100 microns.

As shown in Fig. 32, photoresist 304 is next deposited and patterned to allow for etching of the metal interconnecting lines of the invention, 306, as shown in Fig. 33. Etching of the bulk metal 302 and underlying adhesion layer 300 can be performed by dry or wet etching, as is known in the art. Referring to Fig. 34, the photoresist 304 is stripped. Subsequent metal layers may be formed in a similar manner to that shown for the first metal layer in Figs. 30-34. For example, referring to Fig. 35, another thick polymer layer 308 is deposited over the interconnect line 306 and an opening 310 formed for connection of the next metal layer to the first metal layer. Adhesion and bulk metal layers are then sputtered as described above, a photoresist deposited and patterned, metal etching performed, etc.

Referring now back to Fig. 1, the tops 9 of the top metal conductor can now be used for connection of the IC to its environment, and for further integration into the surrounding electrical circuitry. Pads 10, 11 and 12 are formed on top of the top 9 of the metal conductors 7; these pads can be of any design in width and thickness to accommodate specific circuit design requirements. A larger size pad can, for instance, be used as a flip chip pad. A somewhat smaller in size pad can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in Fig. 1: pad 10 can serve as a flip chip pad, pad 11 can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical signal bus, pad 12 can also serve as a flip chip pad. There is no connection between the size of the pads shown in Fig. 1 and the suggested possible electrical connections for which this pad can be used. Pad size and the standard rules

and restrictions of electrical circuit design determine the electrical connections to which a given pad lends itself.

The following comments relate to the size and the number of the contact points 6, Fig. 1. Because these contact points 6 are located on top of a thin dielectric (layer 3, Fig. 1) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad 6 small. The size of pad 6 is however also directly related with the aspect ratio of via 7. An aspect ratio of about 5 is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad 6 can be in the order of 0.5 um. to 3 um. the exact size being dependent on the thickness of layers 4 and 5.

The present invention does not impose a limitation on the number of contact pads that can be included in the design; this number is dependent on package design requirements. Layer 4 in Fig. 1 can be a typical IC passivation layer.

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer 4, a layer of approximately 0.2 um. PECVD oxide is deposited first followed by a layer of approximately 0.7 um. nitride. Passivation layer 4 is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron

process (of the interconnecting metallization structure) is of critical importance since it allows for a cheaper process that possibly has less stringent clean room requirements for the process of creating the interconnecting metallization structure.

In addition to PECVD oxide and PECVD nitride, passivation layer 4 may also be formed of silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), or combinations thereof.

Layer 5 is a thick polymer dielectric layer (for example polyimide) that has a thickness in excess of 2 um (after curing). The range of polyimide thickness can vary from 2 um. to 50 um. dependent on electrical design requirements. The polymer layer 5 is thicker than the intermetal dielectric layers in the interconnecting, fine-line, metallization structure by 2 to 500 times.

For the deposition of layer 5 the Hitachi-Dupont polyimide HD 2732 or 2734 can, for example, be used. The polyimide can be spin-on coated and cured. After spin-on coating, the polyimide will be cured at 400 degrees C. for 1 hour in a vacuum or nitrogen ambient. For thicker polyimide, the polyimide film can be multiple coated and cured.

Another material that can be used to create layer 5 is the polymer benzocyclobutene (BCB). This polymer is at this time commercially produced by for instance Dow Chemical and has recently gained acceptance to be used instead of

typical polyimide application. Yet other possible materials for layer 5 include a silicone elastomer, paralyne, or parylene.

The dimensions of opening 7 have previously been discussed. The dimension of the opening together with the dielectric thickness determines the aspect ratio of the opening. The aspect ratio challenges the via etch process and the metal filling capability. This leads to a diameter for opening 7 in the range of approximately 0.5 um. to 3.0 um. while the height for opening 7 can be in the range of approximately 3 um. to 20 um. The aspect ratio of opening 7 is designed such that filling of the via with metal can be accomplished. The via can be filled with CVD metal such as CVD tungsten or CVD copper, with electro-less nickel, with a damascene metal filling process, with electroplating copper, etc.

It must be noted that the use of polyimide films as inter-level dielectrics has been pursued as a technique for providing partial planarization of a dielectric surface. Polyimides offer the following characteristics for such applications:

- they produce surfaces in which the step heights of underlying features are reduced, and step slopes are gentle and smooth.
- they are available to fill small openings without producing the voids that occur when low-temperature CVD oxide films are deposited.
- the cured polyimide films can tolerate temperatures of up to 500 degrees C. without degradation of their dielectric film characteristics.

- polyimide films have dielectric breakdowns, which are only slightly lower than that of SiO_2.
- the dielectric constant of polyimides is smaller than that of silicon nitride and of SiO_2.
- the process used to deposit and pattern polyimide films is relatively simple.

For all of the above characteristics, polyimides are used and recommended within the scope of the present invention.

Fig. 2 shows how the present invention as indicated in Fig. 1 can be further extended to include multiple layers of polyimide and, in so doing, can be adapted to a larger variety of applications. The lower level build up of this cross section is identical to the build up shown in Fig. 1 with a silicon wafer 1, the poly silicon layer 2, the metal and dielectric combined layer 3, the passivation layer 4, the polyimide layer 5 and the pads 10 deposited on top of layer 5. The function of the structure that has been described in Fig. 1 can be further extended by depositing another layer of polyimide 14 on top of the previously deposited layer 5 and overlaying the pads 10. Selective etching and metal deposition can further create contact points 12. These contact points 12 can be connected with pads 10 as shown by connector 13. Depositing pads 12 on top of layer 14 can thus further extend this process. These pads 12 can be further customized to a particular application, the indicated extension of multiple layers of polyimides greatly enhances the flexibility and usefulness of the present invention. Additional alternating layers of polyimide and metal lines and/or power or ground planes may be added

above layers 12 and 16, as needed. Contact between metal layers formed in the post passivation method of the invention can be made by direct contact between two layers of metal (as shown in Fig. 12), or alternately by metal plugs formed in the openings between metal layers.

The polymer layers 14 that are formed between the thick, post-passivation metal lines are formed to a thickness of between about 2 and 30 microns, after curing, and are thicker than the intermetal dielectric layers formed in the typical fine-line metal scheme (layers 3) by a ratio of between about 2 and 500. The thicker, organic polymer used in the post-passivation process of the invention reduces capacitance between the thick metal lines. The inorganic materials, such as silicon oxide, used in the fine-line metallization system 3, cannot be formed to such thicknesses due to a tendency to crack at these thicknesses.

Figs. 3a and 3b show a top view of one possible use of the present invention. Interconnecting a number of pads 32 that have been created as described creates signal lines 30. Additional contact points such as point 34 can allow signal lines to pass vertically between layers. The various contact points can, for instance, be created within the surface of a power plane or ground plane 36. The layers within the interconnecting metallization structure of the present invention can contain signal interconnections in the X-direction, signal interconnections in the Y-direction, signal interconnections between X and or Y directions, interconnections to and/or within power and/or ground buses. The present invention further teaches the interconnection

of signal lines, power and ground buses between the connected IC's and the top of the metallization system of the present invention.

Fig. 3a shows signal lines formed in the X-direction, Fig. 3b shows signal lines formed in the Y-direction.

Fig. 4 presents yet another application of the present invention. Shown in Fig. 4 is an exploded view of a part of

Fig. 5 that presents an area array I/O distribution. Fig. 4 shows pads 41 (on which solder bumps can be created) and an example of a layout of the redistribution of the peripheral pads 41'. The exploded view of Fig. 4 is taken along the line 2-2' shown in Fig. 5, the redistribution of the peripheral pads 41' (see Fig. 4) is, for clarity of overview, not shown in Fig. 5. The power or ground connections can be made to any point that is required on the bottom device. Furthermore, the power and ground planes can be connected to the power and ground planes of the package substrates. Fig. 4 shows an example of how to use the topmost metal layer to redistribute the peripheral pads 41' to become area array pads 41. The solder bumps can then be created on pads 41.

Fig. 5 shows the top surface of a plane that contains a design pattern of a combination of power or ground pads 52 and signal pads 54. Fig. 5 shows the pad openings in the top dielectric layer. It is to be noted that the ground/power pads 52 are heavier and larger in design relative to the signal pads 54. The present invention ideally lends itself to meeting these differences in design, as

they are required within the art of chip and high performance circuit design. The number of power or ground pads 52 shown in Fig. 5 can be reduced is there are power and/or ground planes within the chip. From this it is clear that the package number of I/O's can be reduced within the scope of the present invention which leads to a reduction of the package cost by eliminating common signal/power/ground connections within the package. For instance, a 470 I/O count on a BGA chip can, within the scope of the present invention, be reduced to a 256 I/O count using the present invention. This results in considerable savings for the overall package.

Fig. 6 shows a basic design advantage of the invention. This advantage allows for the sub-micron or fine-lines, that run in the immediate vicinity of the metal layers 3 and the contact points 6, to be extended in an upward direction 20 through metal interconnect 7'. This extension continues in the direction 22 in the horizontal plane of the metal interconnect 26 and comes back down in the downward direction 24 through metal interconnect 7". The functions and constructs of the passivation layer 4 and the insulating layer 5 remain as previously highlighted under Fig. 1. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micron and sub-micron level to a metal interconnect level that has considerably larger dimensions and is therefore characterized by smaller resistance and capacitance and is easier and more cost effective to manufacture. This aspect of the invention does not include any aspect of conducting line re-distribution and therefore has an inherent quality of simplicity. It

therefore further adds to the importance of the invention in that it makes micron and sub-micron wiring accessible at a wide-metal level. The interconnections 7' and 7" interconnect the fine-level metal by going up through the passivation and polymer or polyimide dielectric layers, traverses over a distance on the wide-metal level and continues by descending from the wide-metal level back down to the fine-metal level by again traversing down through the passivation and polymer or polyimide dielectric layers. The extensions that are in this manner accomplished need not to be limited to extending fine-metal interconnect points 6 of any particular type, such as signal or power or ground, with wide metal line 26. The laws of physics and electronics will impose limitations, if any, as to what type of interconnect can by established in this manner where limiting factors will be the conventional limiting factors of resistance, propagation delay, RC constants and others. Where the invention is of importance is that the invention provides much broader latitude in being able to apply these laws and, in so doing, provides a considerably extended scope of the application and use of Integrated Circuits and the adaptation of these circuits to a wide-metal environment.

Fig. 7 shows how the basic interconnect aspect of the invention can further be extended to now not only elevate the fine-metal to the plane of the wide-metal but to also add power, ground and signal distribution interconnects of power, ground and signal planes at the wide-metal level. The wide-metal interconnect 26 of Fig. 6 is now extended to further include an interconnection with the via 21. In typical IC design, some pads may not be positioned in a location from which easy fan-out can be accomplished to a location that is required for the next step of circuit assembly. In

those cases, the BGA substrate requires additional layers in the package construction in order to accomplish the required fan-out. The invention teaches an approach that makes additional layers in the assembling of an IC feasible while not unduly increasing the cost of creating such a multi-layer interface. Ball formation 28 on the surface of interconnect 23 indicates how the invention replaces part of the conventional BGA interconnect function, the solder bump provides for flip chip assembly. This interconnect 28 now connects the BGA device with surrounding circuitry at the wide-metal level as opposed to previous interconnects of the BGA device at the fine-metal level. The wide-metal interconnect of the BGA has obvious advantages of cost of manufacturing and improved BGA device performance. By being able to readily extend the wide-metal dimensions it also becomes possible to interconnect power, ground and signal lines at a wide-metal level thereby reducing the cost and complexity of performing this function at the fine-metal level. The indication of 28 as a ball does not imply that the invention is limited to solder bumps for making interconnects. The invention is equally applicable to wirebonding for making circuit interconnects.

Fig. 8 further shows a cross section wherein the previous linear construction of the metal interconnection running through the passivation layer and the insulation layer is now conical in form. The sub-micron metal layer 60 is covered with a passivation layer 62, a layer 64 of polyimide or polymer is deposited over the passivation layer 62. The wide metal level 66 is formed on the surface of layer 64. The via 70 is shown as having sloping sides, these sloping sides can be achieved by controlling the photolithography process that is used to created the via 70. The etching of the

polyimide or polymer can for instance be done under an angle of about 75 degrees with the following curing being done under an angle of 45 degrees. Also, a photosensitive polyimide or polymer can be used, the cone shape of the via 70 can in that case be achieved by variation of exposure combined with time of exposure combined with angle of exposure. Where non-photosensitive polymer or polyimide is used, a wet etch can be applied that has a gradated faster and longer time etch as the top of the via 70 is being approached. The layer of wide-metal pad 68 is deposited on the surface of the polymer or polyimide layer 64, the wide-metal pad deposition 68 mates with the top surface of the via 70 and is centered on top of this surface.

Figs. 9 through 11 show further detail to demonstrate the concepts of BGA chip ball fan-out, pad relocation and the creation of common ground, power and signal pads.

Fig. 9 shows a cross section 100 of a BGA chip, five balls 101 through 105 are also shown. By using the BGA substrate 106 and the wiring 107 within the substrate 106, it is clear that ball 101 can be repositioned to location 111, ball 102 to location 112, etc. for the remaining solder bumps 103 through 105. It is clear that the separation of contact points 111 through 115 is considerably larger than the separation of the original solder bumps 101 through 105. The BGA substrate 106 is the subject of the invention, this substrate allows for spreading the distance between the contact points or balls of the BGA device to a considerable degree.

Fig. 10 shows the concept of pad relocation. BGA pad 120 can be any of the contact balls 101 through 105. By using the BGA substrate 130 and the wiring 131 that is provided within the substrate, it is clear that the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging. For instance contact point 101, which is on the far left side of the BGA device 100, is re-routed to location 121 which is on the second far right of the BGA substrate 130. The re-arrangements of the other BGA solder bumps can readily be learned from following the wiring 130 within the substrate 131 and by tracing from solder bump to one of the contact points 122 through 125 of the BGA substrate.

Fig. 11 shows the interconnecting of BGA device solder bumps into common power, ground or signal pads. The BGA chip 100 is again shown with five solder bumps 101 through 105. The BGA substrate 130 contains a wiring scheme that contains in this example three wiring units, one for each for the power, ground and signal bumps of the BGA device. It is clear from Fig. 11 that wire arrangement 132 connects BGA device solder bumps 101, 103 and 105 to interconnect point 138 of the BGA substrate 130. It can further be seen that BGA device solder bump 104 is connected to interconnect point 140 of the BGA substrate by means of the wire arrangement 136, while BGA device solder bump 102 is connected to interconnect point 142 of the BGA substrate by means of the wire arrangement 134. The number of pins required to interconnect the BGA device 100 is in this manner reduced from five to three. It is clear that for more BGA device solder bumps, as is the case for an actual BGA device, the numeric effect of the indicated wiring arrangement is considerably more beneficial.

The concept of pad relocation can be realized using the metal interconnection scheme described in this invention, to replace the function of BGA substrate 130. From Figs. 10 and 11 it can be seen that the extended functionality and extended wiring ability that are provided by the interconnect wiring schemes that are typically created in the BGA substrate 130 can be created using the method of the invention, on device 100. Some of the methods and possibilities of interconnect line routing that can be implemented using the method of the invention are highlighted in the following paragraphs.

Fan-out capability can be provided by the invention, using the metal conductors within the openings through the insulating layer and through the passivation layer that connect electrical contact pads of the top metallization structure with contact points of the interconnecting metallization structure. Each of the electrical contact points of the interconnecting metallization structure is connected directly and sequentially with at least one electrical contact point of the top metallization structure. In a fan-out scheme, the distance between electrical contact points of the top metallization structure is larger than the distance between electrical contact points of the interconnecting metallization structure by a measurable amount.

The number of electrical contact pads of the upper metallization structure can exceed the number of contact points of the interconnecting metallization structure by a considerable amount.

Pad relocation may also be accomplished by the method of the invention. Electrical contact points of the top metallization structure are connected with the contact points of the interconnecting metallization structure, directly but not necessarily sequentially, thereby creating a pad relocation effect. In this method, the distance between electrical contact points of the top metallization structure is larger than the distance between the electrical contact point of the interconnecting metallization structure by a measurable amount.

A reduction effect may also be accomplished by the method of the invention, wherein common nodes are connected together. Electrical contact points on a top surface of the top metallization structure are connected with contact points of the interconnecting metallization structure, where fewer contact points are used in the top metallization structure, since functionally equivalent contact points in the interconnecting metallization structure are connected together. That is, the number of contact points for a particular electrical function among the electrical contact points of the top metallization structure is smaller than the number of electrical contact points of the interconnecting metallization structure by a measurable amount.

Some of the advantages of the present invention are:

1) improved speed of the IC interconnections due to the use of wider metal lines (which results in lower resistance) and thicker dielectrics between the interconnecting lines

(which results in lower capacitance and reduced RC delay). The improved speed of the IC interconnections results in improved performance of High Performance IC's.

2) an inexpensive manufacturing process since there is no need for expensive equipment that is typically used in sub-micron IC fabrication; there is also no need for the extreme clean room facilities that are typically required for sub-micron manufacturing.

3) reduced packaging costs due to the elimination of the need for redundant I/O and multiple power and ground connection points that are needed in a typical IC packaging.

4) IC's of reduced size can be packaged and inter-connected with other circuit or system components without limiting the performance of the IC's.

5) since dependence on ultra-fine wiring is reduced, the use of low resistance conductor wires is facilitated.

6) structures containing more complicated IC's can be created because the invention allows for increased I/O pin count.

7) more complicated IC's can be created without the need for a significant increase in re-distribution of package I/O connections.

8) power buses and clock distribution networks are easier to integrate within the design of IC's.

9) future system-on-chip designs will benefit from the present invention since it allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

10) form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

11) provide a means to standardize BGA packaging.

12) be applicable to both solder bumps and wirebonding for making further circuit interconnects.

13) provide a means for BGA device solder bump fan-out thereby facilitating the packing and design of BGA devices.

14) provide a means for BGA device pad relocation thereby providing increased flexibility for the packing and design of BGA devices.

15) provide a means for common BGA device power, ground and signal lines thereby reducing the number of pins required to interconnect the BGA device with the surrounding circuits.

16) provide a means for more relaxed design rules in designing circuit vias by the application of small passivation (0.1 um or more) vias.

17) provide the means for extending a fine-wire interconnect scheme to a wide-wire interconnect scheme without the need to apply a passivation layer over the surface of the fine-wire structure.

Although the preferred embodiment of the present invention has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.